# System-on-chip Sensor Fusion Front-End Self-Healing Design for Network-on-Chip Digital Communications

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*Abstract*— **With the ultra-scaling of CMOS technology, high-speed and low-power millimeter-wave communication systems for network-on-chip have been attracting more and more attentions due to the wider bandwidth and higher data rate that can meet the ever-increasing needs for multimedia, massive external data storage, or even biomedical applications. However, from manufacturing's perspective, the circuits implementations are increasingly susceptible to fabrication process variations with the scaling of CMOS technology, which results in loss of yield rate. To solve this issue, a sensor-fusion solution is proposed in this paper by adding multiple on-chip sensors, including power detectors, temperature sensors, information envelope detectors and related filters, instrumentation amplifiers using a standard CMOS process. These sensors and detectors aim to collect critical system performance and environmental parameters, which will be utilized by a self-healing and optimization algorithm to adjust the state of system components by digitized control knobs.**

*Index Terms* — **network-on-chip, high-speed communication, system-on-chip, sensor fusion**

## I. INTRODUCTION

The ultra-scaling CMOS technology leads chips, printed circuit boards (PCBs), modules, and servers to moving towards higher data rates and smaller form factor [1-5]. With faster switching speed of single transistors, CMOS technology enables many applications, including radio-frequency wireline [6-8] or wireless communication [9-12], navigation systems [13], human-machine interface [14-16], mm-wave technology [17-20] and even THz technology [21-23].

High-speed millimeter-wave communication systems have been attracting attention because of the wider bandwidth and higher data rate that can meet the ever-increasing needs for multimedia applications. In the past, radio systems developed for such a broad frequency range have been made of discrete III-V compound MMICs with relatively high component and system costs and long development time. However, a standard CMOS process is being widely discussed in developing low-power and low-cost radio-on-chip (RoC) for multi-Gbps wireless communications, which can offer cost-effective manufacturing with the highest integration capability for both digital and mixed signal circuits. The device scaling of CMOS technologies improves the performance of the transistors in terms of a higher unity gain frequency and maximum frequency

of oscillation. In other words, the transistor speed increases, so does the operation frequency. However, unfortunately, the use of scaled CMOS technologies also poses daunting technological challenges both in design and manufacturing test. From circuit designer's point of view, the deeply-scaled CMOS process (65nm and below) produces extra design challenges as the following: (1) The supply voltage has to be lower and therefore causing a more constrained signal dynamic range and linearity; (2) The metal density requirements become more stringent along with the thinner dielectric layers above the substrate will lead to higher substrate losses of passives and therefore a lower gain and output power.

From manufacturing's perspective, the circuits concerned are increasingly susceptible to manufacturing process variations with the scaling of CMOS process, which results in loss of manufacturing yield. The effects of such process variations on the performance of high speed mixed-signal/RF circuitry manufactured using deeply scaled CMOS technology is particularly severe, requiring the use of post-manufacture tuning for yield recovery.

This work, as part of the self-healing transceiver project, focus on the sensor and instrumentation frond-end circuit design, which include power detector, envelope detector, temperature sensor, analog multiplexer, anti-aliasing filter and instrumentation amplifier. These sensors and detectors aim to detect the critical circuit overall performance and the environmental parameter, such as temperature, IM3 component, P1dB point. Then detected information will be send to optimization algorithm to adjust the state of RX and TX circuit after being digitized by auxiliary ADC.

## II. DEVICE SCALING AND CMOS PROCESS VARIATION



Fig. 1 Examples of process variation

Fig. 1 shows some examples of CMOS fabrication fluctuations that fundamentally cause process variation. In general, there are four types of variations: lot-to-lot variation, wafer-to-wafer variation, die-to-die variation, and within-die variation. Die-to-die and within-die variations have significant

impacts on the circuit performance and power consumption. With continuing scaling of CMOS technology, process variation is even more pronounced because transistor geometry and threshold voltage variations become a considerable fraction of their nominal values.
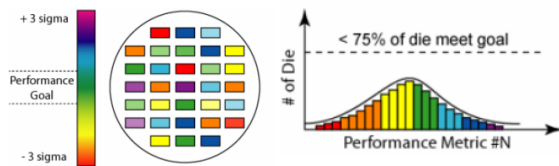


Fig. 2 Process variation and yield loss

The immediate drawback of process variation is yield-loss. Without process variation, the yield should be 100% if the circuit is designed properly. However, with process variation, the circuit performance of chips becomes a random variable with a certain distribution, which is illustrated in the left plot in Fig. 2. Other technologies may also experience severe variations at even less aggressive nodes. Therefore, there will be some point that process variation reduces all the benefits resulting from process scaling. To combat process variation, novel system architecture and design methodologies are essential.

### III. SELF-HEALING ARCHITECTURE WITH SENSOR FUSION

Process variation becomes an increasing issue in the super-scaled CMOS design as mentioned above. The traditional method used in the analog/RF design sector to battle process variation is known as the corner-based design. It means that the circuit is over-designed with enough performance margins in the typical case such that it satisfies all of the specifications in the worst corner. This methodology has been widely used in the industry since it guarantees robustness. However, the drawback is its implementation cost. This is because large amount of silicon area and power dissipation have to be invested just to accommodate the worst-case corner. Such design approach is not very efficient, since the worst-case corner does not happen very often in practice. Most of the chips are in the typical corner; therefore, the large silicon real-estate and disproportionally high power dissipation can become quite wasteful. A more efficient design methodology should be developed to focus on meeting the specifications in the typical corner so that silicon area and current consumption requirements are relaxed and dynamically adapt the circuits in other corners where the specifications are not met. An innovative concept of self-healing is proposed to enable this feature.

Figure 3 shows the block diagram of the proposed self-healing reconfigurable CMOS radio-on-a-chip. It consists of two parts: baseline and self-healing. The baseline circuits that are required for normal radio operation are marked in white while the self-healing overheads that are added to enable the healing capability are marked in green. On the transmitting side, the transmitter chain first starts off with the quadrature

10-bit I/Q DAC that convert the digital signals into analog ones. Afterwards, the analog signals will be low-pass filtered by a pair of quadrature low-pass filters (LPFs). After low-pass filtering, the quadrature signals are up-converted from baseband to 12 GHz by a pair of IF quadrature mixers. The four quadrature phases at the outputs of the IF quadrature mixer are phase combined to become differential.
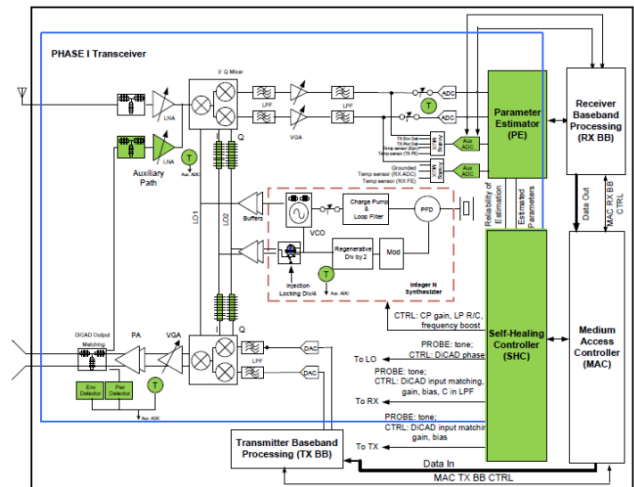


Fig. 3 System diagram of the self-healing reconfigurable radio

On the receiving side, the received signal is first amplified by a low-noise amplifier (LNA) that operates at 60 GHz. It is then downconverted from 60 GHz to 12 GHz by a RF mixer. The downconverted signal at 12 GHz is then downconverted to baseband by a pair of quadrature IF mixers. This particular type of transceiver architecture is also known as the "sliding-IF" architecture. After the signal is downconverted to baseband, a pair of quadrature LPFs and programmable-gain amplifiers are used to further condition the signal before it is digitized by the signal-path ADC.

### IV. SELF-HEALING PROCESS AND SENSOR FUSION BUILDING BLOCK DESIGN

#### A. Self-healing Process Control

At start-up and stand-by periods, self-healing is activated periodically to sense and adjust the radio so the optimal performance can be maintained. The healing does not affect the normal operation of the radio. The worst case combined yield is less than 45%. The vision is to design an integrated radio with 75% performance yield in the presence of extreme process and environmental variations with novel circuit design techniques and control algorithms while the area and power overheads are minimized (< 10%).
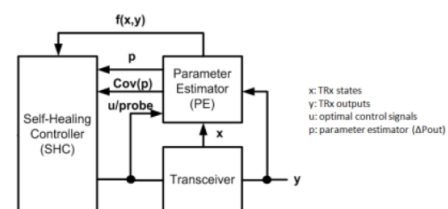


Fig. 4 Self-healing control architecture

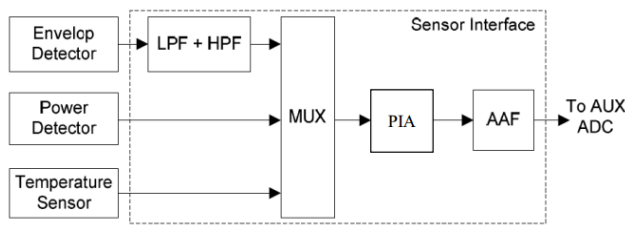## B. Multiple Sensing Front-end Architecture


Fig. 5 Sensors and instrumentation front-end block

The self-healing overheads include an auxiliary ADC, temperature detectors, power detectors, envelope detector, programmable gain amplifiers (PGAs), multiplexers (MUXs), and healing control application-specific integrated circuits (ASICs), as Fig. 5 shown. The healing control components consist of self-healing controller, ADC control unit, calibration unit, DAC control unit, SRAM lookup table, clock divider, and offline testing unit. The detectors are dedicated to sense the states of the baseline transceiver. The temperature detector is used to monitor the on-chip temperature variation so receiver noise can be estimated. The power and envelope detectors are used to capture the transmitted output power and envelope so they can be used to obtain transmitter impairments such as LO leakage, I/Q mismatch and image, and to estimate the gain of the receiver with the closed-loop calibration. The outputs of the detectors are amplified and connected to a 4-to-1 MUX prior to a PGA. The MUX selects among the outputs of temperature detectors, power detector, and envelope detector and forwards the selected signal to be digitized by an auxiliary ADC. The speed of the auxiliary ADC is much slower (10 MS/s) and its size is much smaller than the signal-path ADC. Various amplifiers with programmable gain are used to maximize the dynamic range of the auxiliary ADC. Self-healing controller adjusts various components in the transceiver according to this information provided by detector to compensate the performance deviation in the presence of environmental and process variations.

## C. Building Blocks Design

The temperature sensors are used to provide relative temperature change information to the healing controller during the tracking mode, which are placed at multiple different locations on the system-on-chip. The specification for the temperature sensors is shown in Table 1. The placements of the

| Parameters | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|
| Supply | 0.9 | 1.0 | 1.1 | V | |
| Temperature Range | 10 | | 100 | C | |
| Resolution | | | 5 | C | |
| Output | 1 | | | V | Peak-to-peak differential |
| Relative Error | | 1 | | C | |
| Area | | | 0.05 | mm$^2$ | |
| Power | | | 2 | mW | |
| Power down (PD) Control bit | 1 | 1 | 1 | bit | Active low: '0' -> power down '1' -> power up |
| Wakeup time | | | 0.1 | us | Bias level to 95%. |
| Sleep time | | | 0.1 | us | Bias level to 5%. |

Table 1 Temperature sensor specifications
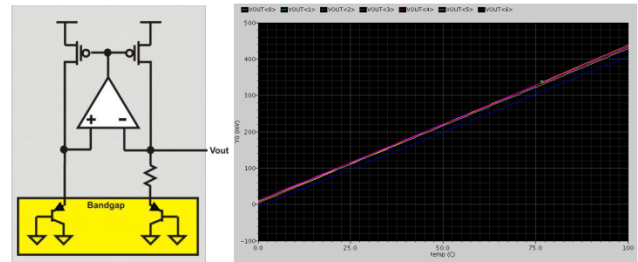
temperature sensors are shown in Fig. 6.


Fig. 6 Temperature sensor and simulation of sensor across process corners

The transmitter power detector is used to provide a closed loop power control locally at the transmitter by detecting the transmitted output power level at the PA and feeding this detected output power in a voltage reading to the ADC. The digitized detector reading is then used by the SH controller to adjust the output power of the power amplifier to meet a given output power requirement, as shown in Fig. 7.
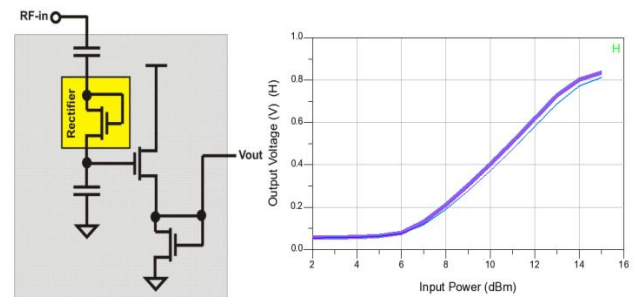

Fig. 7 Power detector and simulation of sensor across process corners

An envelope detector takes a high-frequency signal as its input and provides the envelope of the signal as its output. It is widely used for gain control and spectral energy estimation. A robust envelope detector is necessary as part of the instrumentation system to improve the overall circuit performance yield. For a complete closed-loop self-healing function, the envelope detector attached to transmitter output detects the impairments of the baseline transmitter, as shown in Fig. 8. Fig. 9 shows the physical layout implementation on
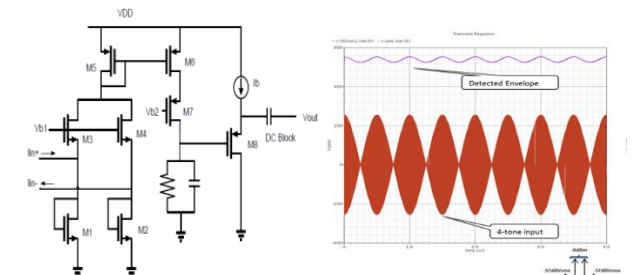

Fig. 8 Envelope detector and simulation of sensor across process corners

TSMC 65nm CMOS technology.

## V. CONCLUSION

In this paper, three different levels of broadband communication channels are discussed through chip-to-chip, board-to-board, and server-to-server, from bottom to top. We

overview the common electrical characteristics, power, and signal integrity. Table I compares the performance differences of different generations in terms of data rate, energy efficiency, electrical characterisicts.
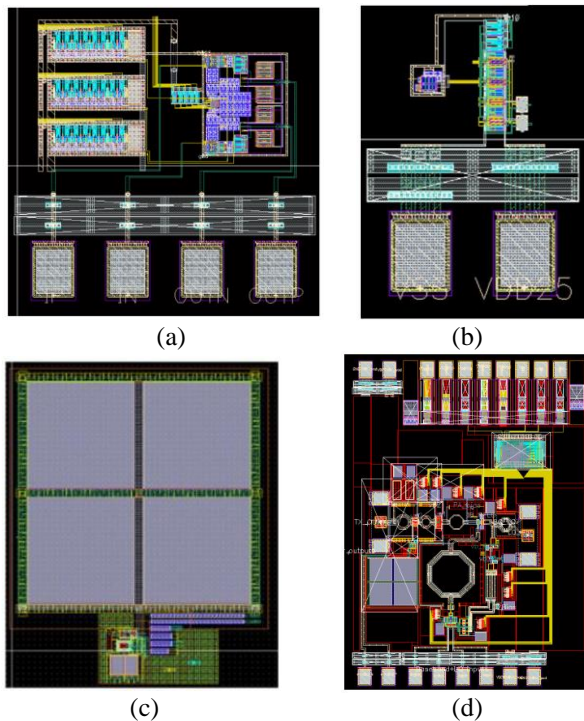


(a)  (b)

(c)  (d)

Fig. 8 TSMC 65nm CMOS technology implementations (a) temperature sensor with instrumentation amplifier, (b) power detector, (c) envelope detector, (d) Integrated with power amplifier

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