A Viterbi decoder and its hardware Trojan models: An FPGA-based implementation study

Varsha K[1]**, Karthi Balasubramanian**[1]**, B.Yamuna**[1]**, Deepak Mishra**[2]**,**
Karthikeyan Lingasubramanian[3]**, and Senthil Murugan**[4]

[1]**Department of Electronics and Communication Engineering, Amrita School of**
Engineering, Coimbatore, Amrita Vishwa Vidyapeetham, India
[2]**Digital Communication Division (DCD), Optical and Digital Communication Group**
(ODCG), Satcom Navigation Payload Area (SNPA), Space Application Center (SAC),
ISRO, Ahmedabad, India
[3]**Electrical and Computer Engineering, University of Alabama at Birmingham, USA**
[4]**Department of Electronics and Communication Engineering, Amrita School of**
Engineering, Amritapuri, Amrita Vishwa Vidyapeetham, India

Corresponding author:
Karthi Balasubramanian[1]

Email address: b_karthi@cb.amrita.edu

ABSTRACT

Integrated circuits may be vulnerable to hardware Trojan attacks during its design or fabrication phases. This paper is a case study of the design of a Viterbi decoder and the effect of hardware Trojans on a coded communication system employing the Viterbi decoder. Design of a Viterbi decoder and possible hardware Trojan models for the same are proposed. An FPGA-based implementation of the decoder and the associated Trojan circuits have been discussed. The noise-added encoded input data stream is stored in the block RAM of the FPGA and the decoded data stream is monitored on the PC through an UART interface. The implementation results show that there is barely any change in the LUTs used (0.5%) and power dissipation (3%) due to the insertion of the proposed Trojan circuits, thus establishing the surreptitious nature of the Trojan. In spite of the fact that the Trojans cause negligible changes in the circuit parameters, there are significant changes in the bit error rate (BER) due to the presence of Trojans. In the absence of Trojans, BER drops down to zero for SNRs higher than 6 dB, but with the presence of Trojans, BER doesn't reduce to zero even at a very high SNRs. This is true even with the Trojan being activated only once during the entire duration of the transmission.

Keywords Coded communication system, Viterbi decoder, Hardware Trojan, Bit error rate.

INTRODUCTION

The entry of connected technologies into the realms of Internet of Things (IoT) and Cyber Physical Systems (CPS) has made it imperative for communications systems to be protected from possible threats. These threats can arise from both software externals and hardware internals. While considerable emphasis is being given to software level threats, in this work we focus on the hardware level threats. The hardware of a communication system can be compromised if its design is exposed so that it can be modified or duplicated. This allows an adversary to deteriorate the performance of a communication system and expose the system to attacks. This makes understanding of the hardware level threats significant. In this work, we focus on the effect of one such threat called hardware Trojans, on coded communication systems that use a Viterbi decoder as the error correcting unit.

Overview of coded communication system

Design of efficient coder-decoder (CODEC) for error control has received increased interest in recent years. This is due to the fact that all digital transmission and storage requires error control strategy to ensure reliability. Information symbols from a source are encoded by the addition of controlled redundancy. Convolutional codes and block

45 codes are the broad classification of error control codes. An error control decoder makes the best estimate of the
46 transmitted codeword by making use of the redundancy added at the encoder. The transmitted codewords are encoded
47 information symbols that are subject to errors, in the process of transmission through noisy communication channels.
48 These transmitted codewords can be decoded with as low bit error rate as possible for transmission rates upto the
49 channel capacity (Sweeney, 2002). The block level representation of a coded communication system is shown in
50 supplementary figure 1.

Hardware Trojans

52 In the current scenario of integrated circuits (ICs) manufacturing, a globalized business model has emerged where
53 ICs are manufactured in foundries that are distributed in various parts of the world. A hardware Trojan is a malicious
54 stealthy modification that leads to malfunctioning of the system (Colins, 2007). Such modifications in the system
55 provides a back door entry for the Trojans. The three main categories of hardware Trojans are based on their action,
56 physical and activation characteristics (Chakraborty et al., 2009; Tehranipoor and Koushanfar, 2010; Karri et al.,
57 2010a; Banga et al., 2008; Ranjani and Devi, 2017). The physical characteristics category describes the various
58 hardware manifestations of Trojans according to their shape and size; the activation characteristics describe the
59 conditions that activate the Trojans and action characteristics refer to the behavior of the Trojans. Supplementary
60 figure 2 gives the classification of Trojans based on insertion phase, abstraction level, activation mechanism and
61 effects.

62 Hardware Trojans can be inserted at different stages of IC design cycle, while the most prevalent phases are
63 design and fabrication. Likewise, Trojans can be realized at different levels of IC design abstraction and can be
64 designed to get triggered internally by specific states of the system, or externally through any communication medium.
65 The former can be stealthy based on the occurrence of the problem states, while the latter will be untraceable in
66 test phase because it is not triggered internally. Regarding the effect of Trojans on the affected system, they are
67 generally designed by the adversary to change functionality or leak sensitive information or deny service during
68 critical instances or compromise the communication system and reduce the reliability of the design (Karri et al.,
69 2010b).

70 There are numerous post manufacturing techniques for detecting Trojans but a single technique is difficult to
71 be devised for detecting Trojans universally. Side channel and logic testing form the two classical Trojan detection
72 techniques (Narasimhan et al., 2013). In these two methods, a golden circuit is used to compare with outputs of the
73 circuit under test. Typically, Trojans are devised to activate rarely to escape logic testing and evade detection. They
74 also possess small physical characteristics to evade side channel based testing.

Trojan modelling

76 Trojans are generally modelled for the specific design of interest that they intended to disrupt. Examples of Trojan
77 benchmark circuits aimed at infecting systems like advanced encryption system (AES), serial interface RS232,
78 Ethernet MAC, 8051 and PIC microcontrollers can be found at (TrustHUB, 2019). These circuit models have been
79 widely used to study the effectiveness of Trojan infection and to design measures to thwart them. To study the Trojan
80 effect on other systems, custom Trojan models are designed. A few studies that have been done in recent years on a
81 system level using custom Trojan models are listed below:

82 • Saeidi and Garakani (2016): Multiple hardware Trojans have been designed for a 256x128 array of 6-transistor
83 SRAM block, that either corrupt the output or modify the delay and duty cycle of the enable signals. The
84 Trojans are trigged by an address sequence that is not generally produced in conventional testing methodology,
85 thereby helping them to evade detection by conventional SRAM testing.

86 • Tiwari et al. (2019): A hardware Trojan model has been proposed for launching denial of service attack to
87 on-chip multicast routing algorithms. The Trojan is modelled to use the on-chip temperature sensor information
88 to identify suitable nodes and launch attack on multicast data packets.

89 • Liu et al. (2016): The design and custom silicon implementation of secret key leaking Trojans present in
90 the ultrawide band transmitter of a wireless cryptographic IC has been presented. The Trojan circuit leaks
91 the encryption key without disrupting the normal operation. This is achieved by hiding the key in the power
92 amplitude and frequency margins that are acceptable due to process variations.

93 • Kumar et al. (2018): Novel hardware Trojans are proposed that induces denial of service and performance
94 degradation in a Network on Chip. The Trojan is triggered by a complex bit pattern generated from input
95 messages, intended towards misleading the packets away from the destination address.

96 • Subramani et al. (2019): Hardware Trojan attack is modelled by modifying the encoder block of a 802.11a/g
97 transmitter. This is accomplished by hijacking some of the legitimately encoded bits and substituting with
98 rogue bits.

Trojan modelling of channel decoders

Channel decoders are a quintessential part of any coded communication system. They are soft targets for Trojan attacks and can be embedded with malicious blocks for the following reasons: (Hemati, 2016).

- They have a direct interface with the outside world that make them susceptible to being hijacked.

- They process noisy information that makes it impossible for a even a perfectly functional decoder to be successful all the time. Hence a Trojan affected system may easily claim false failures and masquerade its real purpose.

- Brute force approach of running all test cases to identify malicious activity is not practical with even a medium size block length since the number of input and output combinations will be huge.

In spite of the fact that channel decoders are highly susceptible to Trojan attacks, the effects of Trojans on them hasn't been explored in literature. Hemati et al. in (Hemati, 2016) have proposed the use of stochastic techniques at a system level for mitigating Trojan effects in a channel decoder but an RTL level analysis is missing. Our work involves the proposal and analysis of possible Trojans on a specific channel decoder namely, the Viterbi decoder. The work is concentrated towards RTL design of a Viterbi decoder and possible Trojans that may potentially compromise the communication system and reduce the reliability of the decoder.

Viterbi algorithm is widely used for decoding convolutional codes since it achieves maximum likelihood estimate of the convolutionally coded transmitted sequence (Forney, 1973). A low bit error rate (BER) can be achieved by a Viterbi decoder (Viterbi, 1967). However the presence of Trojans can affect the performance of the decoder significantly. This has been demonstrated with a proof of concept in our earlier work (Aravind et al., 2018). Trojan models were proposed and behavioral modeling studies at the algorithmic level showed that the BER performance of convolution decoder using the Viterbi algorithm is degraded due to the presence of the hardware Trojans. The current work extends this proof of concept to a RTL level circuit design of the decoder and the Trojan activities. A practical implementation of the Viterbi decoder is achieved and the Trojan effects on the system is analyzed.

The paper is organized as follows. The Viterbi decoder section details the reader about the Viterbi algorithm with a suitable example. This is followed by the section on the hardware design of the decoder for FPGA implementation. Results from simulation and FPGA implementation of the decoder are discussed after that, followed by the section on the design of the Trojans. Results and discussions on the Trojan based design are presented and the paper then concludes with references to possible future work.

VITERBI DECODER

The n encoded output in a (n,k,m) convolutional code depends on the k present input blocks as well the m past input blocks. A memory m sequential circuit is used for realizing the convolutional encoder. The trellis diagram of the rate half, $m = 2$, convolutional encoder is shown in figure 1. Supplementary figure 3 shows the corresponding state diagram of the trellis.
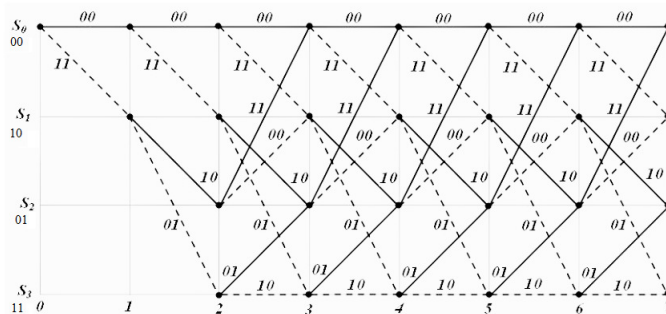
Figure 1. Trellis structure of the convolutional encoder

The state transitions and the outputs reached in response to changes in input are represented in the state diagram. In the trellis diagram the same information is described in stages which represent the different time instants. With states representing the past memory contents of the encoder and branches representing the state transitions, the trellis path traced by the Viterbi decoder is a sequence of branches. The input message bit corresponding to each branch in the sequence of branches represent the decoded message sequence. By adding terminating zeros to the message sequence it is ensured that the decoder always starts in an all-zero initial state for decoding a message sequence. A detailed example showing the decoding procedure may be found in the supplementary document.

FPGA BASED VITERBI DECODER DESIGN

The Viterbi decoder was designed in Verilog and implemented on a Xilinx Zybo-Z7010 board. Figure 2 shows the top level implementation structure that includes the core decoder block, a single port block RAM (BRAM) of size 8x1024 to store the input data and a single port block RAM of size 8x512 to store the decoded data. Along with these, an UART transmitter module is also integrated to monitor the decoded data on a PC.
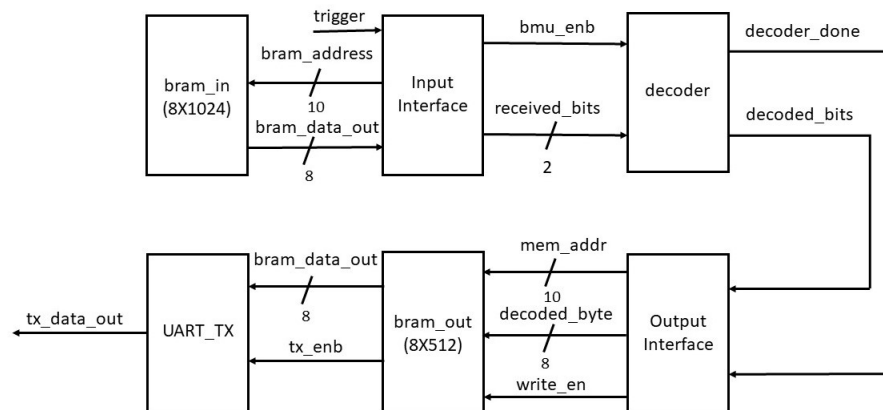
Figure 2. Block level diagram for FPGA implementation of Viterbi decoder

Input Interface

The noise added encoded message is stored in the input BRAM and data is transferred to the decoder block through the input interface. The interface logic unit consists of a counter and an 8 bit shit register as shown in figure 3.
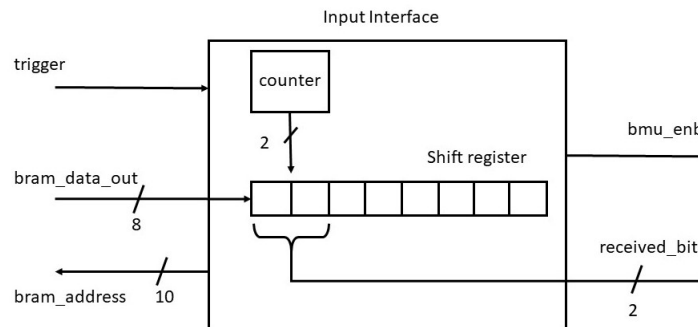
Figure 3. Input interface

It reads the data byte-wise from the BRAM and transmits 2 bits per clock cycle to the decoder block for further processing. At every clock cycle two LSB bits are shifted out to the BMU block. After every four clock cycles, the subsequent BRAM location is read and processed similarly.

Decoder design

Figure 4 shows the top level block diagram of the decoder consisting of the branch metric unit (BMU), path metric unit(PMU), survivor path memory unit (SPMU), spmu_controller and the trace back unit(TBU).

Branch metric and path metric units

The BMU calculates the Hamming distance between the received frame and the branch word while the PMU performs add-compare-select calculations as described in (Middya and Dhar, 2016). Figures 5 and 6 show the blocks used for the Hamming distance calculation and the ACS (add-compare-select) units.

During every clock cycle, BMU calculates the eight branch metrics corresponding to the two transitions of each of the four states. The branch metrics are then passed on to the PMU that updates each state with the least path metric corresponding to each of the states and also stores the corresponding path leading to it in the form of a 'decision bit',
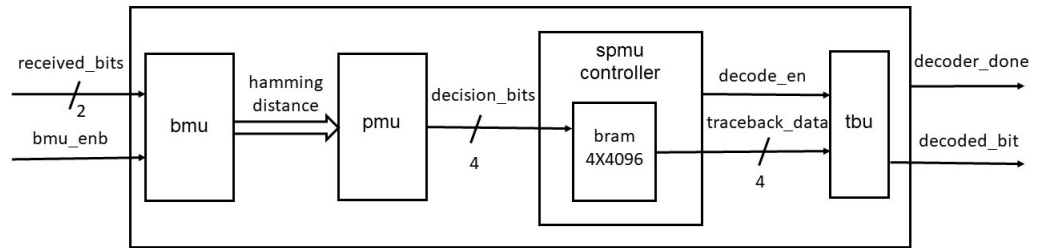
Figure 4. Decoder block diagram
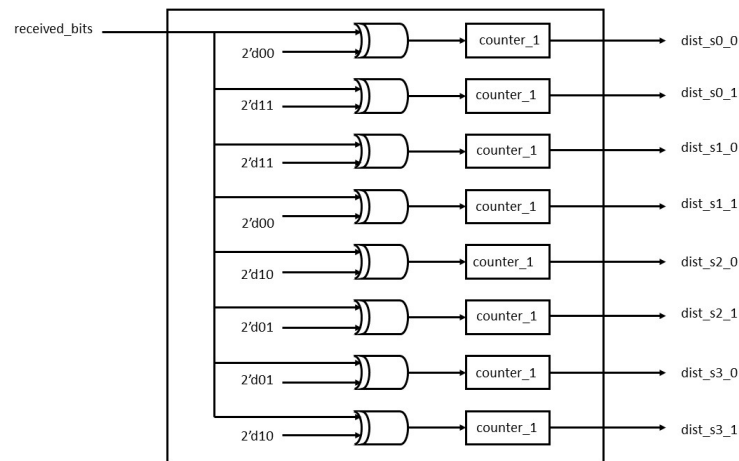
Figure 5. Hamming distance unit
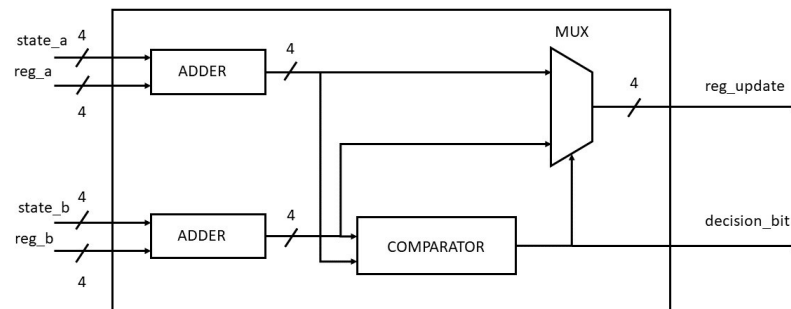
Figure 6. Add carry select block

one for each of the 4 states at every time instant. It can be seen from the trellis diagram in figure 1 that each state has two incoming paths. The decision bit is set to '0' if the state is reached from the top branch while it is set to '1' if it is reached from the bottom branch. Figure 7 shows the block diagram of the PMU block to update the path metrics and for decision bit calculations for the four states.

Survivor path memory unit (SPMU) and trace back unit (TBU)

Survivor path memory is designed as a single port BRAM that stores the decision bit values of all states at each of the time instants. The structure of the SPMU is the same as the trellis structure shown in figure 1. For the input data size of 1024 bytes, the number of decision bits generated would be 4096 for every state. Thus a 4x4096 BRAM is used as the SPMU. The SPMU_update module reads the decision bits from the PMU block and updates the SPMU every clock cycle. This continues till the SPMU is populated with all the 4x4096 decision bit values. Once the SPMU is populated with the decision bits, the decode_en bit is triggered high and the trace back unit kicks in to start the reverse process to decode the original input bits. Figure 8 shows the state machine used for the trace back operation.

Since the encoded message is terminated with zeros, the final state of the system would be the zero state and
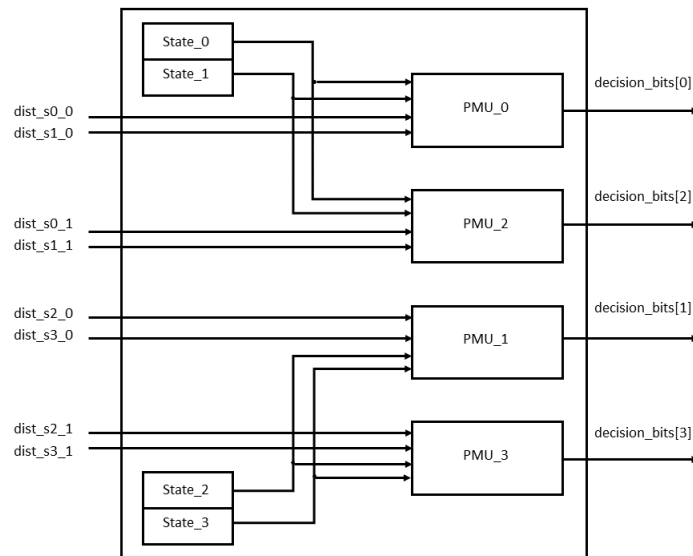
Figure 7. PMU blocks for all the four states
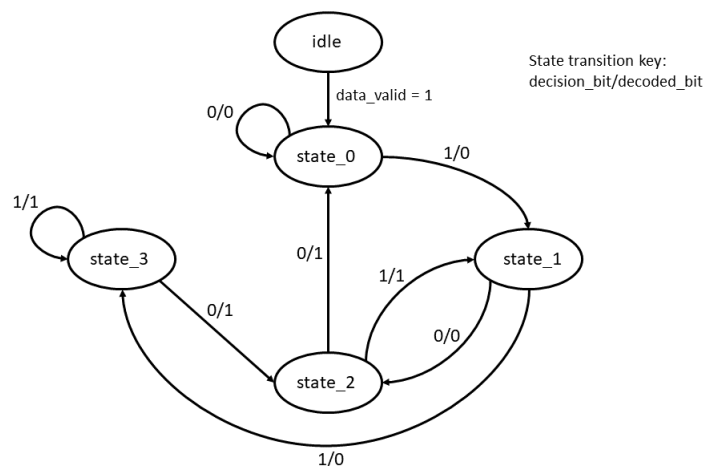
Figure 8. State transition diagram of the trace back Unit (TBU)

177 hence TBU can be safely initialized to start the decoding from the zero state. After decoding all the 4096 bits,
178 decode_done signal is activated to trigger the output interface. It is to be noted that it takes around 4096 clock cycles
179 for the forward tracing, 4096 clock cycles for traceback and few cycles are required for synchronization.

180 ***Output Interface***
181 The output interface consists of a first-in-first-out (FIFO) buffer of size 8x512 (4096 bits) to store the decoded data
182 and the baud generator and transmitter modules of universal asynchronous receiver transmitter (UART) to transmit
183 the data serially on to a PC. The UART is designed with a frame length of 10 (1 start bit, 8 data bits and one stop bit)
     and works at a baud-rate of 9600 bps. Figure 9 shows the UART frame used in the design.
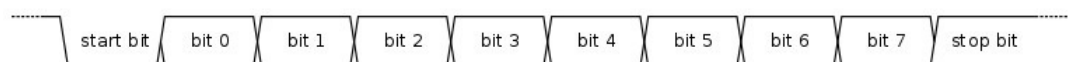
Figure 9. 10 bit UART Frame

184

185 The data from the decoder is first stored in the FIFO and is transmitted when an external request for data transfer
186 is enabled. The FIFO is designed using a BRAM of size 8x512. FIFO is chosen to be one byte wide to enable byte
187 wise data transfer to the UART transmitter easily. Figure 10 shows the transmitter block designed to operate at a baud
188 rate of 9600 bps.
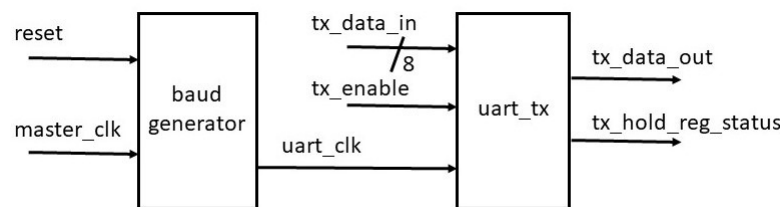
Figure 10. UART Transmitter

189

The UART transmitter contains the baud generator that generates the UART clock corresponding to a baud rate
of 9600 bps. To generate this clock from the master clock, we use a clock divider whose value can be obtained by
using equation (1)

$$Baudrate = \frac{master\_clk}{(16 \times divisor)} \qquad (1)$$

190 Since the master clock of the FPGA board (Zybo Z7010) is 125 MHZ, we need to design a clock divider of value
191 given by equation (2)

$$divisor = \frac{master\_clk}{(16 \times Baudrate)} = 813.4 \qquad (2)$$

192 Rounding off to the nearest highest integer, we use a clock divider of value 814 to generate the UART clock and
193 data is transmitted out serially to the PC through a RS232 interface .

SIMULATION AND IMPLEMENTATION OF VITERBI DECODER

Input data generation

196 A coded communication system is set up as detailed in the introduction section, using MATLAB. 4K message bits are
197 generated randomly and encoded using a convolutional encoder of rate $\frac{1}{2}$ to generate 8K encoded bits. Binary phase
198 shift keying (BPSK) modulation is used to modulate the encoded message stream and the resulting data sequence is
199 transmitted through an additive white gaussian noise (AWGN) channel of varying signal to noise rations (SNRs). The
200 received sequences are demodulated and stored as inputs for the Viterbi decoder.

Design and functional verification

202 The Viterbi decoder was first designed using a behavioral model in MATLAB and then a synthesizable RTL design
203 was done in Verilog. The original encoded message sequence (without noise addition) is given as input to the decoders
204 and the output was verified to be the original message sequence. This establishes that the decoders are functionally
205 correct. Having verified the functionality of the designs using the encoded message as the inputs, the noise-added
206 sequences are given as inputs and the bit error rates are computed.

FPGA Implementation

208 The RTL design of the decoder was synthesized on to a Zybo board that is built using Z-7010, a member of Xilinx
209 Zynq-7000 family. Z-7010 is designed using Xilinx all programmable system-on-chip architecture (AP SoC), that
210 integrates a Xilinx 7-series FPGA along with an ARM based Cortex-A9 processor. In our work, we have not used
211 the ARM processor for generating test inputs but instead, the test vectors are generated from MATLAB as briefed
212 above and a single port BRAM is initialized with these input test vectors. The decoded output bits are first stored in
213 another BRAM and then sent by the UART transmitter to the PMOD pins of the Zybo board. This transmitted data is
214 driven through a UART-to-USB translator (PL2303) and the serial bits are captured on the PC using Real Term serial
215 terminal (RealTerm, 2019).

216 Functional verification of the implemented design was done in the same manner as the simulated design. The
217 encoded message bits without noise addition were given as the input and the decoded bits were compared with
218 the original message sequence. It was verified that the decoded and input message bits matched successfully. For
219 calculating the decoder performance, the decoder was fed with noisy data of different SNRs.

²²⁰ Figure 11 shows the BERs obtained for the MATLAB behavioral model, the RTL design and the FPGA
²²¹ implementation where it can be seen that the BER drops down to zero for SNRs greater than 6 dB[1]. Also, there is
²²² a perfect overlap of all the plots, thus demonstrating the equivalence of the behavioral, RTL and the implemented
²²³ models.
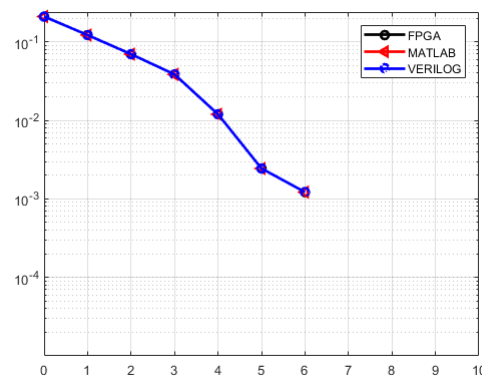
Figure 11. Comparative BER plots for Matlab behavioral design, RTL design and the FPGA implementation (beyond 6 dB, the BER is zero). All three plots overlap perfectly, thus establishing the correctness of the implementation.

²²⁴

TROJAN DESIGN AND IMPLEMENTATION

²²⁶ In this work, we propose the design of three possible Trojans and study how their stealthy presence may affect the
²²⁷ system performance.

Trojan Design 1: Decision-bit flipping Trojan (PMU Trojan)

²²⁹ In the Path metric unit (PMU), it is expected that the comparator identifies the least path metric path and corre-
²³⁰ spondingly store a '1' or '0' to indicate either of the paths to be traversed during trace back. The proposed Trojan
²³¹ *Decision-bit flipping*, when enabled, flips the decision bits thus causing the trace back unit to proceed in an incorrect
²³² decoding path. The hardware model of the Trojan circuit is shown in figure 12.
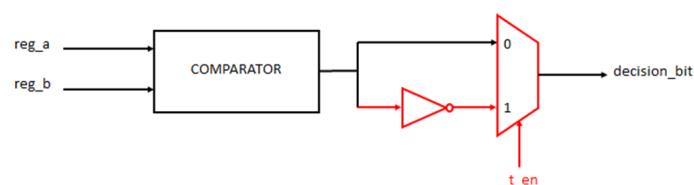
Figure 12. PMU Trojan

²³³

²³⁴ The decision bit is inverted when Trojan is enabled and the SPMU gets populated with an incorrect value. This
²³⁵ causes the lower metric path to be discarded instead of the higher path metric, thus resulting in possible erroneous
²³⁶ decoding.

Trojan Design 2: Traceback path modification Trojan (TBU Trojan)

²³⁸ During trace back, the decision bits from the SPMU is read and a path is chosen based on whether the stored value is
²³⁹ a '0' or a '1'. The *traceback path modification* Trojan inverts this logic and changes the state transitions, thus making
²⁴⁰ it proceed in the wrong path. Figure 13 shows the modified state machine due to the Trojan being effective.
²⁴¹ When the Trojan is enabled, the transitions are made to differ from the original state transitions resulting in
²⁴² erroneous decoding.

---

[1]Since the BER is plotted on a log scale, it is not possible to indicate the zero values on the plot
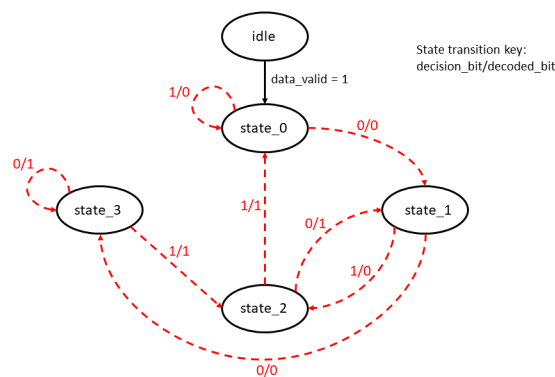
Figure 13. Trojan effect modifying the trace back path in the TBU

Trojan Design 3: Shift-direction-modifying Trojan

In the output interface, when the decoded data is being written into the shift register, normally it will be right shift operation. But when the Trojan is enabled this operation will be reversed and performs left_shift thus sending erroneous data to the transmitter. This can be achieved by the use of multiplexers that can alter the shift direction based on the Trojan enable signal. Figure 14 shows the Trojan circuitry that is created due to this Trojan.
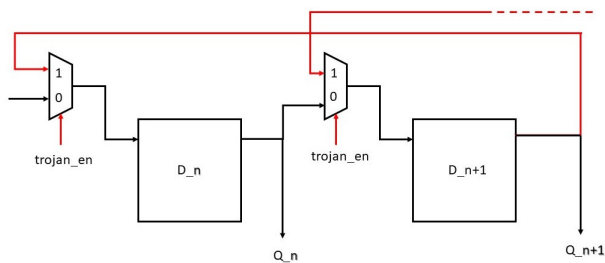
Figure 14. Shift direction modifying Trojan

RESULTS AND DISCUSSIONS

The effectiveness of the designed Trojans can be gauged by their stealthy nature and by their propensity to degrade the performance of the infected system.

Stealthy Trojans

Trojans by nature are stealthy in nature and are difficult to detect. To verify if the proposed Trojan models are stealthy enough to evade detection, the difference in the area and power dissipated due to the Trojan insertion are calculated. Tables 1 and 2 show the power and utilization summary of the Trojan free circuits and the Trojan affected circuits. It is to be noted that the parameters obtained is only for the decoder logic without including the input BRAM and the output UART.

Table 1. Power Summary Table

Power Summary (W)	Without Trojan	PMU Trojan	TBU Trojan	Shift modification Trojan
Total on-chip power	0.129	0.129	0.133	0.13
Dynamic	0.025	0.025	0.03	0.026
Device static	0.104	0.104	0.104	0.104

It can be seen from the power and area utilization results that in the worst case, there is a difference of only 4 mW of on-chip power (difference of 3.1%), and only 4 extra LUTs (change of 0.5%) due to the Trojan insertions. This establishes its stealthy nature, thus qualifying them as effective Trojans.

Table 2. Utilization Summary Table

Utilization		Without Trojan		PMU Trojan		TBU Trojan		Shift modification Trojan	
Site Type	Available	Used	Util%	Used	Util%	Used	Util%	Used	Util%
Slice LUTs	17600	453	2.57	451	2.56	457	2.59	455	2.58
LUT as Logic	17600	197	1.11	195	1.1	201	1.14	199	1.13
LUT as Memory	6000	256	4.26	256	4.26	256	4.26	256	4.26

Performance degradation

To analyse how effectively the Trojans disrupt the natural decoding process, the Trojans are triggered at random time instants and the decoded bits are analyzed. Generally, Trojans are designed to activate surreptitiously in order to go unnoticed. Hence the triggering was done only once during the entire decoding process and the effect of this triggering is observed and the resultant BER is calculated.

Trojan triggering Logic

Figure 15 shows the circuit for generating Trojan enable signal. It consists of a BRAM, a 14 bit counter to count up to the maximum possible number of clock cycles required for decoding and a comparator. The Trojan can be triggered any time during the entire duration of decoding. To identify these triggering instances, 50 random numbers are generated and stored in a block RAM. During each triggering one location is read from the BRAM as the triggering instance. The Trojan enable signal is generated when the counter value matches with the random number being read from the BRAM. The BER is calculated to be the average of the BERs obtained from all the triggering instances.
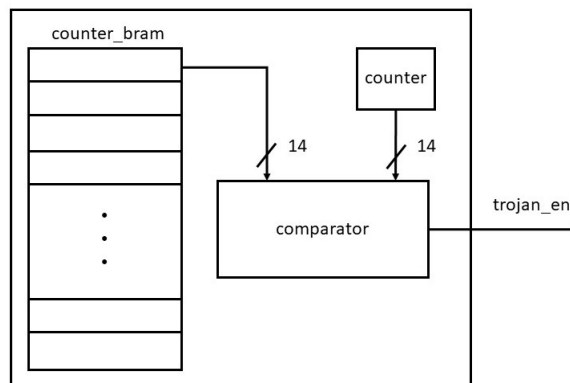
Figure 15. Trojan triggering logic

Effect of the triggered Trojans

The effect of the Trojans may be quantified by the increase in the bit error rates of the infected decoder. Figures 16-18 show the comparative BER graphs of the decoder without Trojan and with Trojan being activated only once.

It can be seen that in the absence of Trojans, the BER drops down to zero for SNRs greater than 6 dB, but with the Trojans being active, the BER doesn't reduce to zero even for high SNRs. Thus the Trojans leave a distinctive BER signature (high BER). Among the three Trojans, the BER signature is highest for TBU Trojan and lowest for PMU Trojan, with the shift modification Trojan producing a BER signature in between the other two.
It is also interesting to note that the difference in the performances between the Trojan free design and the design with Trojans is negligible in the low SNR regions but the difference is prominent in the high SNR regions. Also at some low SNR conditions, the performance of the Trojan affected system is slightly better than the unaffected system. This scenario is possible since, in the low SNR regions, the data itself is noisy and erroneous. During the bit flipping or the state transition or the shift direction modifying actions of the Trojans there exists a possibility that few erroneous bits are converted to correct bits, thus providing a reverse effect on the system. The possibility of this kind of behaviour, along with the fact that Trojans are stealthy make it difficult to conjure effective Trojan detection schemes. To counter such situations, the current focus of researchers is to neutralize them apart from detecting the Trojans (Gunti and Lingasubramanian, 2017).
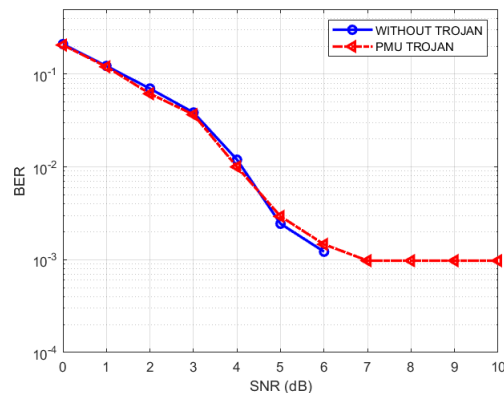
Figure 16. BER plot for PMU Trojan
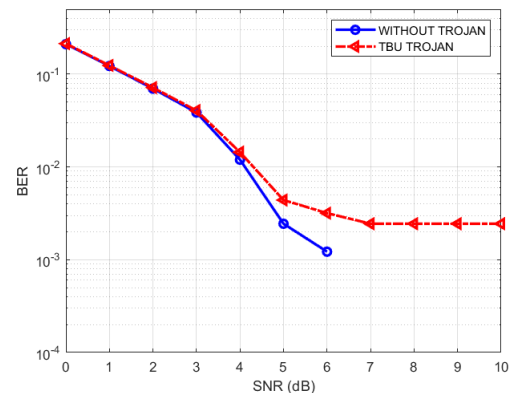
Figure 17. BER plot for TBU Trojan
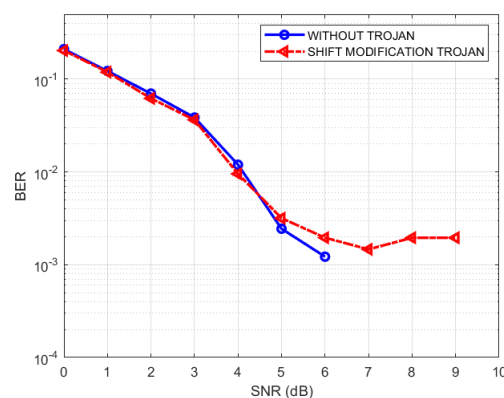
Figure 18. BER plot for shift direction modifying Trojan

Study Limitations

The study proposes stealthy Trojans- *decision bit flipping, traceback path modification and shift direction changing* Trojans- and their effect on the decoding efficiency of a Viterbi decoder. The Trojans degrade the performance of the decoder, causing it to have a high BER. But, it is to be noted that high BER can also arise in a system due to high noise in the channel. Hence in situations where the channel's noise characteristics are unknown, the presence of these Trojan can't be inferred purely from the BER signature. It needs to be augmented with other Trojan detection schemes to correctly infer the presence of Trojans.

CONCLUSIONS

In this work, we have designed a FPGA based implementation of a Viterbi decoder and presented possible effects of hardware Trojans on coded communication systems. Three unique threat models are developed and tested on the Viterbi decoder which is popular for its low BER performance. However, we show that the presence of the proposed Trojans affect the efficiency of the Viterbi decoder by increasing the BER. The stealthiness of the proposed Trojans is also established. Using the proposed threat models, we envision to test their effects on complex systems like CPS and IoT which rely on efficient communication channels.

With the wide application of convolution codes in various SNR scenarios, the results of the implemented system play a significant role in emphasizing the need for efficient Trojan detection schemes. It is envisaged that apart from BER signature analysis, other Trojan detection and neutralizing schemes will be explored for the proposed Trojans.

REFERENCES

Aravind, A. R., Kesavaraman, S. R., Balasubramanian, K., Yamuna, B., and Lingasubramaniam, K. (2018). Effect of hardware trojans on the performance of a coded communication system. In *2018 IEEE International Conference on Consumer Electronics (ICCE)*, pages 1–6.

310 Banga, M., Chandrasekar, M., Fang, L., and Hsiao, M. S. (2008). Guided test generation for isolation and detection of
311   embedded trojans in ics. In *Proceedings of the 18th ACM Great Lakes symposium on VLSI*, pages 363–366. ACM.

312 Chakraborty, R. S., Narasimhan, S., and Bhunia, S. (2009). Hardware trojan: Threats and emerging solutions. In
313   *High Level Design Validation and Test Workshop, 2009. HLDVT 2009. IEEE International*, pages 166–171. IEEE.

314 Colins, D. (2007). Trust in integrated circuits (tic). *DARPA Solicitation BAA07-24*.

315 Forney, G. D. (1973). Convolutional codes 11. maximum-likelihood decoding. *Information and Control*, 25(3).

316 Gunti, N. B. and Lingasubramanian, K. (2017). Effective usage of redundancy to aid neutralization of hardware
317   trojans in integrated circuits. *Integration*, 59:233–242.

318 Hemati, S. (2016). Mitigating hardware cyber-security risks in error correcting decoders. In *2016 9th International
319   Symposium on Turbo Codes and Iterative Information Processing (ISTC)*, pages 181–185. IEEE.

320 Karri, R., Rajendran, J., Rosenfeld, K., and Tehranipoor, M. (2010a). Trustworthy hardware: Identifying and
321   classifying hardware trojans. *Computer*, 43(10):39–46.

322 Karri, R., Rajendran, J., Rosenfeld, K., and Tehranipoor, M. (2010b). Trustworthy hardware: Identifying and
323   classifying hardware trojans. *Computer*, 43(10):39–46.

324 Kumar, M., Swain, A. K., Kumar, S., Sahoo, S. R., and Mahapatra, K. (2018). Run time mitigation of performance
325   degradation hardware trojan attacks in network on chip. In *2018 IEEE Computer Society Annual Symposium on
326   VLSI (ISVLSI)*, pages 738–743. IEEE.

327 Liu, Y., Jin, Y., Nosratinia, A., and Makris, Y. (2016). Silicon demonstration of hardware trojan design and detection in
328   wireless cryptographic ics. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, 25(4):1506–1519.

329 Middya, A. and Dhar, A. S. (2016). Real-time area efficient and high speed architecture design of viterbi decoder.
330   In *Advances in Electrical, Electronics, Information, Communication and Bio-Informatics (AEEICB), 2016 2nd
331   International Conference on*, pages 246–250. IEEE.

332 Narasimhan, S., Du, D., Chakraborty, R. S., Paul, S., Wolff, F. G., Papachristou, C. A., Roy, K., and Bhunia, S.
333   (2013). Hardware trojan detection by multiple-parameter side-channel analysis. *IEEE Transactions on computers*,
334   62(11):2183–2195.

335 Ranjani, R. S. and Devi, M. N. (2017). Malicious hardware detection and design for trust: an analysis. *Elektrotehniski
336   Vestnik*, 84(1/2):7.

337 RealTerm (2019). Serial/TCP Terminal. *Available at `https://sourceforge.net/projects/realterm/`
338   (accessed 23 April 2019).

339 Saeidi, R. and Garakani, H. G. (2016). Sram hardware trojan. In *2016 8th International Symposium on Telecommuni-
340   cations (IST)*, pages 719–722. IEEE.

341 Subramani, K. S., Antonopoulos, A., Abotabl, A. A., Nosratinia, A., and Makris, Y. (2019). Demonstrating and
342   mitigating the risk of a fec-based hardware trojan in wireless networks. *IEEE Transactions on Information
343   Forensics and Security*.

344 Sweeney, P. (2002). *Error Control Coding: From Theory to Practice*. John Wiley & Sons, Inc., New York, NY, USA.

345 Tehranipoor, M. and Koushanfar, F. (2010). A survey of hardware trojan taxonomy and detection. *IEEE design & test
346   of computers*, 27(1).

347 Tiwari, B., Yang, M., Jiang, Y., and Wang, X. (2019). Effect of hardware trojan attacks on the performance of on-chip
348   multicast routing algorithms. In *2019 IEEE 9th Annual Computing and Communication Workshop and Conference
349   (CCWC)*, pages 0623–0629. IEEE.

350 TrustHUB (2019). Trojan Benchmarks. *Available at `https://trust-hub.org/benchmarks/trojan`
351   (accessed 15th August 2019).

352 Viterbi, A. (1967). Error bounds for convolutional codes and an asymptotic optimum decoding algorithm. *IEEE
353   Transactions on Information Theory*, 13(2).