Review
Teaching computer architecture by designing and simulating processors from their bits and bytes

The paper describes the practical elements of an interesting course in computer architecture.
Tasks include processor instruction and architecture design, HDL capture and HDL simulation, development of an assembly program simulator,
assembly/test using discrete components.

Abstract: please review, clearly stating the goals of the work, the need for practical application in comp arch, what the students achieved, tools used,
feedback obtained (much is already in abstract)

It would be interesting to capture the duration of the tasks (and sub-tasks), and review the efficiacy of each section.
The discrete components element, which challenging and interesting, may be the least efficient element.

It would also be very interesting to obtain student feedback using surveys
Specify the university program, module title, duration of the course, the pre-requisite knowledge, year of course group size

"As expected, when it comes to teaching computer architecture to students, it becomes more challenging since most of them are not interested, since advances in other areas attract them more unsurisingly."
I acceopt this point though believe that it is possible to make comp arch more interesting and accessible, and try to stem the growing lack of interest.
The author's may be interested in reviewing the RIS-C Online Tutor (https://www.vicilogic.com/static/ext/remoteFPGA/vicilogicPublications.html)

Line 122 "As of our knowledge, in the literature, there is no such study to demonstrate the comparison of two different CPU designs proposed by students,
under certain limitations."
Is this a significant point though. It is not clear what exactly the 'two' designs are

Line 132: is given -> are described

Avoid use of 'we' and 'will' throughout
'given' instruction -> 'specified' instruction

Line 147 remove 'recruitments'?
Consider removing 'The problem was simple' -> the specification is to
were -> are

Line 153: not sure that the 16-bit vs 32-bit is worth too much focus.

Line 159: first mention of multiply. Introduce earlier. Also described at line 207.
Sections 2.1, 2.2, 2.3
It would be useful to introduce a diagram of the processor (Figure 2, or simpler) in the intro section, with a short description, with the section 2.1 spec labelled on the diagram
Include a reference to the source of the diagram. Similarly for other diagram sources.
Line 161 2.1 - : remove dash.

'the' MIPS architecutre
R-type register-register?
I-type register-immediate?

Table 1 and Table 2. Is it possible to shorten the interuction desriptions and combine these tables, e.g, like the RISC-V ISA
https://www.vicilogic.com/static/ext/RISCV/riscv-spec.pdf#page=146

Lines 174-185. Reveiw to enhance clarity.

Line 187: provide a similar table format for the syscall and jr instruction

The Group A and Group B text distracts from the paper. Please consider if this A/B requirement could be removed (or alternative names selected), if this could improve paper clarity.
Also, e.g, Fig 5, reference to A/B distracts, particularly since there appears to be only a single simulator.
In this way, just describe the components without refernece to A/B

line 244: classified instruction into two tpyes. I/R have already een introduced (line 166)

line 265: clarify this point

line 268: include a diagram illustrating the points, possibly a common diagram (subset of Fig 1, Fig 3) for several points.

Section 2.3: with a few crafted diagrams, the text could be shorter and more clear.

Line 301 is (delete)

Line 319: state what the simulator is, i.,e, its function and spec first, with diagram.
Section 3: reference a figure with the spec description (even the final version of the simulator). Include (in the diagram) the back-end elements, e.g, assembler)

line 327 Before the CPU design started (remove)
Line 328 MISP - MIPSground - knowledge, assembly programming

line 330 : After the CPU design is complete by the groups, the
331 students created a simulator that supports their own instruction format by making changes to the
332 previous MIPS simulator.
Review clarity of this point.

Similar pint re Group A/B sections/names. Tends to disctract from / complicate the contribution.
Section 3.1/3.2 combine similar elements, with reference to a common well labelled simulator diagram
line 324 : lightened up -> highlighted.

Describe the LCD display. DOes this emulate standard LCD interface signals or is it a software toolbox element?

line 348: They evolved ... simulatro (included details)

Overall comment: future work may be selective on the elements which worked best, to achieve some efficiencies, while allowing students freedome to experiment and be creative.

Section 4
Was an ISE project template provided? Might this be useful. Did the group have experience with the EDA tools? What issues arose.
Line 372: point on ISE/Vivado: I would recommend use of Vivado. Tutorials reference (VHDL)
https://www.vicilogic.com/vicilearn/run_step/?c_id=22&c_pos=31

Section 4.1 description of the processor: can rthis detail be included in the earlier section, with ref to e.g, Figs 1-3. The details seems a bit unnecessary here.
Similar for section 4.2
Again, I make the point re group A/B partitioning distracting from the paper to some extent.
line 409 - all the process is done (review)

line 414 : in a hardware manner (review)

Section 5 seems to be a lot of work!
Section 5.1 what is the outcome?
line 431 plainer circuti (review)
A 4-bit ALU
Is the discrete design the smae as the verilog. If not, this distracts also from the thrust of the paper.
Section 5.1 what is the outcome?
I recommend removal of section 5, since it does not contain results.

Could include syntheses results (resources, speed, RTL schematic diagrams, and consider steps to FPGA implementation.

Discussion section (include section number)
Could rename "Student feedback", though from line 456 is better include in conclusions section
Recommned plot of results (if data is available), listing questions, and drawing conclusions.
The discussion section could be more pecises.

Conclusion (and future work)
Improve quality
e.g, restate the abstract (refer to suggestions earlier
[Abstract: clearly state the goals of the work, the need for practical applciation in comp arch, what the students achieved, tools, feedback]
Recap achievement.
line 488 ... review
line 496 : done - performed
Future work: start the paragraph with "Future work will ..
Ensure that the conclusions section reflects the abstract and is precise and clear

The intro could mirror the reviewed abstract (with more detail)